GUJARAT TECHNOLOGICAL UNIVERSITY, AHMEDABAD, GUJARAT COURSE CURRICULUM

Course Title: Fundamental of Digital Electronics (Code: 3310702)

Diploma Programmes in which this course is offered	Semester in which offered
Computer Engineering, Information Technology,	First Semester
Biomedical Engineering	Second Semester

1. RATIONALE

The objective of Fundamental of Digital Electronics is to make the students understand functioning of a digital circuit. The course contains description of digital components using core structure of digital logic. This includes number system, Logic gates, Boolean algebra, Combinational logic. This Course will enable student to solve various Boolean expressions, to design and implement digital logic circuits.

2. LIST OF COMPETENCIES

The course content should be taught and implemented with the aim to develop different types of skills leading to the achievement of the following competencies.

•Design sequential and combinational circuits of any electronic device.

3. TEACHING AND EXAMINATION SCHEME

Теас	ching S	cheme	Total Credits	Examination Sch			eme	
(In Hou	rs)	(L+T+P)	Theory	Marks	Practica	al Marks	Total Marks
L	Т	Р	С	ESE	PA	ESE	РА	150
3	0	2	5	70	30	20	30	150

Legends: L-Lecture; T – Tutorial/Teacher Guided Theory Practice; P - Practical; C – Credit; ESE – End Semester Examination; PA - Progressive Assessment.

4. DETAILED COURSE CONTENTS

Unit	Major Learning Outcomes	Topics and Sub-topics
Unit – 1: Binary	1.1.Comprehend Number	Binary Systems
Systems	systems and binary codes	Introduction of Digital Computers and
	1.2.Convert Number systems	Digital Systems
	and its complements	Binary Numbers
		➢ Base Conversion
		•BINARY
		•DECIMAL
		•HEX
		•OCTAL
		➤Complements
		•R's Complement
		•2' and 10's Complement
		•(R-1)'s Complement
		•1's and 9's Complement
		1
		➢Binary Codes
		•Decimal Codes
		•Error Detection codes
		Reflected Code
Unit– 2: Binary	2.1.Explain Binary Logic	Binary Logic And Boolean Algebra
Logic And	2.2. List and explain working	Basic Binary logic
Boolean Algebra	of Logic Gates	Logic Gates
	2.3.Solve Boolean algebra	•AND, OR, INVERTER
	2.4.Define and solve various	≻Postulates
	Boolean theorems	≻Boolean algebra
	2.5.Solve Boolean expression	•Two value Boolean algebra
		Basic theorems of Boolean algebra
		De-Morgan's Theorems
		 Boolean functions
		Boolean forms
		•Canonical
		•Standard
Unit-3: Boolean	3.1 Explain Boolean function	Boolean Function Implementation
Function	Implementation and	Need for simplification
Implementation	simplification	\blacktriangleright K – Map method
		●2 – Variable K – map
		•3 – Variable K – map
		●4 – variable K – map
		➤ K – Map using Don't care condition
		 Universal Gates
		•NAND Gate
		•NOR Gate
		 NAND Implementation
		 NOR Implementation

Unit	Major Learning Outcomes	Topics and Sub-topics
Unit- 4: Basic	4.1Explain Basic	Basic Combinational Logic
Combinational	Combinational Logic	 Design procedure of combinational logic
Logic	4.2Design half adder, full	➤ Adder
	adder, Half Subtractor &	•Half Adder
	full Subtractor	•Full Adder
	4.3Explain multiplexer and	> Subtractor
	demultiplexers	•Half Subtractor
		•Full Subtractor
		Code Conversion
		•BCD – Excess-3 conversion
Unit– 5:	5.1Design MSI Combinational	Combinational Logic Using MSI And LSI
Combinational	Logic & LSI	Binary Parallel Adder
Logic Using MSI	5.1 Implement combination	Magnitude Comparator
And LSI	logic circuit using mux	•2 Input Comparator
	and Dmux	> Decoder
		•2 – 4 Decoder
		•3 – 8 Decoder
		≻Encoder
		•4 – 2 Encoder
		•8 – 3 Encoder
		> Multiplexer
		•4 – 1 multiplexer
		Demultiplexers
		•1 – 4 Demultiplexers

5. SUGGESTED SPECIFICATION TABLE WITH HOURS & MARKS (THEORY)

			Distribution of Theory Marks				
Unit	Unit Title	Teaching					
No.		Hours	R	U	Α	Total	
			Level	Level	Level		
1.	Binary Systems	06	2	4	4	10	
2.	Binary Logic and Boolean	08	2	4	6	10	
	algebra					12	
3.	Boolean function	08	4	4	6	1/	
	Implementation					14	
4.	Basic Combinational Logic	10	4	6	6	16	
5.	Combinational Logic Using MSI	10	4	6	8	10	
	and LSI					10	
	Total	42	16	24	30	70	

Legends:

R = Remembrance; U = Understanding; A = Application and above levels (Revised Bloom's taxonomy

6. SUGGESTED LIST OF PRACTICALS

The experiments should be properly designed and implemented with an attempt to develop different types of skills leading to the achievement of the competency.

S. No.	Unit No.	Practical's		
1	1	Convert Number system to another (HEX ,OCTAL,DECIMAL,BINARY)		
2	1	Calculate R's and (R-1)'s Complements		
3	2	Realize the basic logic gates.		
4	2	Realize the NAND gate as a universal building block.		
5	2	Realize the NOR gate as a universal building block.		
6	3	Simplify and design Boolean expression using basic logic gates		
7	3	Simplify and design Boolean expression using Universal gates		
8	4	Design and implement Half Adder and full adder circuit.		
9	4	Design and implement Half Subtractor and full Subtractor circuit.		
10	5	Realize the Binary Parallel Adder circuit		
11	5	Realize Multiplexer and Demultipxer circuit		
12	5	Realize Decoder and Encoder circuit		

7. SUGGESTED LIST OF PROPOSED STUDENT ACTIVITIES

Following is the list of proposed student activities like: course/topic based seminars, internet based assignments, teacher guided self learning activities, course/library/internet/lab based mini-projects etc. These could be individual or group-based.

8. SUGGESTED LEARNING RESOURCES

A. List of Books

S.No.	Author	Title of Books	Publication
1	Mano M. Morris	Digital logic and Computer Design	Pearson publication, Latest Edition ISBN: 81-203-0417-9
2	Jain R.P.	Modern Digital Electronics	Tata McGraw-Hills publication, Latest Edition
3	Malvino & Leech	Digital electronics Principles	Tata McGraw-Hills publication, Latest Edition
4	Anand Kumar	Fundamentals of Digital Circuits	Prentice-Hall of India, Latest Edition

B. List of Major Equipment/ Instrument

- i). Binary to Decimal Converter & Decimal to Binary Converter
- ii). Binary to Gray code Converter & Gray to Binary code Converter
- iii).BCD to Seven Segment Decoder (Common Cathode Display)
- iv).Basic Logic Gates using Diode & Transistor
- v). AND, OR, NOT Gate Characteristics kit
- vi). OR,NOR,EX-OR Gate Characteristics kit
- vii).De-Morgan's Theorem kit
- viii).NAND & NOR as Universal Gate
- ix).Flip-Flop Trainer (D, T, JK, MS Types)

- x). Multiplexer / De-multiplexer using Gates
- xi).Half & Full Adder
- xii).Half & Full Sub tractor
- xiii). A To D Converter using Successive Approximation Method / D to A Converter using Binary Weighed Method (4 bit)
- xiv).Parity Generator / Even & Odd parity Checker
- xv). Bread Board Trainer (For Digital IC's)

C. List of Software/Learning Websites

- i).Digital Electronics Tutorial
- ii). http://www.asic-world.com/digital/tutorial.html

9. COURSE CURRICULUM DEVELOPMENT COMMITTEE

Faculty Members from Polytechnics

- i) M.P.PARMAR, Incharge Head and Senior Lecturer, Information Technology Department, Government Polytechnic, Ahmedabad
- ii)M.D.PATEL, Incharge Head and Senior Lecturer, Information Technology Department Dr. S. S. Gandhy College Surat.

Co-ordinator and Faculty Member from NITTTR Bhopal

- i).Dr.Shailendra Singh, Professor, Dept. of Computer Engineering & Application, NITTTR, Shamla Hills, Bhopal
- ii).Dr.K.James Mathai, Associate Professor, Dept. of Computer Engineering & Application, NITTTR, Shamla Hills, Bhopal